Theory of Logic Circuits					
Academic year	Term	Makrokierunek	Exercise Supervisor	Group	Section
2015/2016	Tuesday 11:45 – 13:15		PCz	1	2

Report from exercise number 3

Exercise performed on: 2016-03-01

Subject of the exercise:

Bistable devices

Section consists of:

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1. Design and implement with NAND gates Sr basic latch with dominant setting input. Draw timing diagrams (taken from the built circuit) illustrating the behaviour of the device.

1.1. Obtained truth table

Q^n	s	r	Q^{n+1}	$Q^{n+1'}$
0	0	0	0	1
0	0	1	0	1
0	1	1	1	1
0	1	0	1	0
1	0	0	1	0
1	0	1	0	1
1	1	1	1	1
1	1	0	1	0

Fig.1. Truth table with expected outputs

1.2. Obtained Karnaugh map

Q^n \ sr	00	01	11	10
0	0	0	1	1
1	1	0	1	1

Fig.2. Karnaugh map based on truth table (Fig.1).

1.3. Equations of the Karnaugh map transformed to fit NAND gates

$$Q^{n+1} = Q^n \cdot \bar{r} \cdot s \Leftrightarrow Q^{n+1} = \overline{\overline{Q^n \cdot \bar{r} \cdot \bar{S}}}$$

$$Q^{n+1'} = \overline{Q^n} \cdot \bar{s} \cdot r \Leftrightarrow Q^{n+1'} = \overline{\overline{\overline{Q^n} \cdot \bar{s} \cdot \bar{r}}}$$

1.4. Circuit

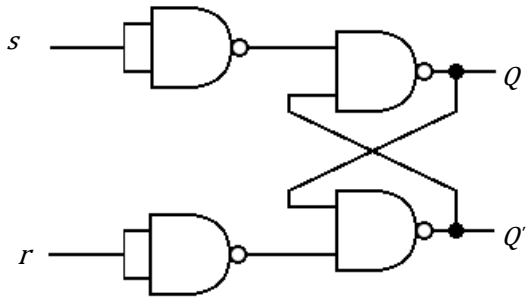

Fig.3. Theoretical circuit

In the laboratory, however, we decided to use complemented inputs rather than complementing NAND gates in the purpose of simplifying the circuit.

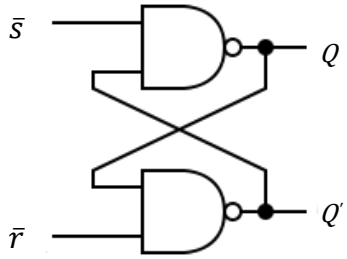

Fig.4. Circuit performed in the laboratory

1.5. Timing diagram

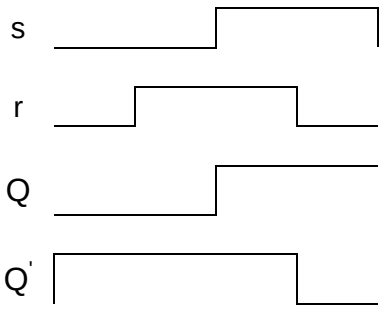

Fig.5. Timing diagram based on the results obtained in the experiment.

2. Recognize the triggering way of the synchronous JK flip-flops (gated latch, master slave with or without 1s and 0s catching, or positive or negative edge-triggered). Draw timing diagrams used to resolve the problem.

   2.1. To simplify the problem exercise was performed on JK flip-flop modified in such a way that we have obtained D flip-flop. The modification did not change the triggering way.

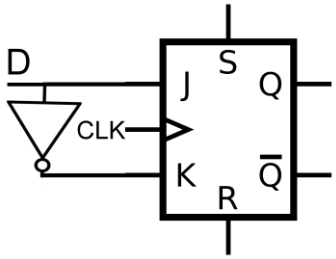

Fig.6. Circuit performed in the laboratory.

   2.2. Dominance of the inputs

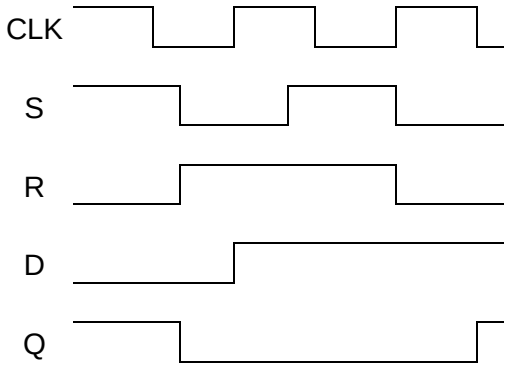

Fig.7. Timing diagram based on the results obtained in the experiment

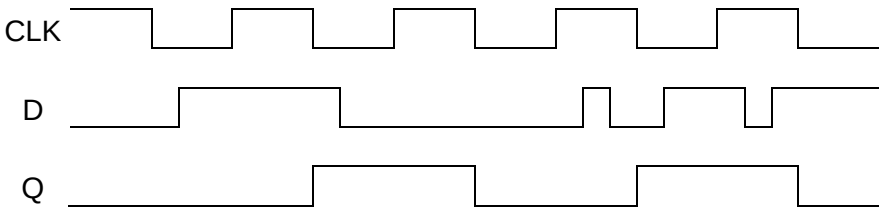

Fig.8. Timing diagram based on the results obtained in the experiment

   2.3. Conclusions

- Set and reset are dominative over D *(Fig.7.)*
- Filp-flop is triggered as master-slave, with both 0's and 1's catching *(Fig.8)*