Theory of Logic Circuits

Academic year	Term		Exercise Supervisor	Deans group	Section
2018/2019	Tuesday 15:00 – 17:45	Makrokierunek	Krzysztof Paszek	1,2	1

Report from exercise number 3

Exercise performed on: 2019-03-06

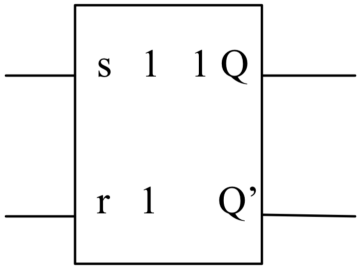
Subject of the exercise:

Bistable devices

Section consists of:
Wojciech Bieniek, gr. 2
Mikołaj Dobosz, gr. 1

Task 1

Design and implement with NAND gates sr basic latch with dominant setting input. Draw timing diagrams (taken from the built circuit) illustrating the behaviour of the device.



Our method:

To start building the gate, we wrote two Karnaugh Maps *q/s/r* for *Q* and *q/s/r* for *~Q*, based on excitation table for SR with S dominance (included in point 1.2 of introductory pdf).

q \ sr	00	01	11	10
00	1	1	1	0
01	0	1	1	0

$$\overline{Q} = r + \overline{q}\,\overline{s}$$ **~Q**

q \ sr	00	01	11	10
00	0	0	1	1
01	1	0	1	1

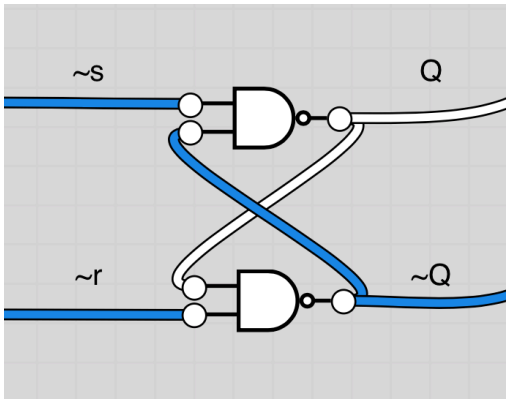
$$Q = q\overline{r} + s$$ **Q**

Next, we had to modify our results to fit it to the lab's equipment. Using double negation and logical transformations, we can compose *Q* and *~Q* of NAND gates.

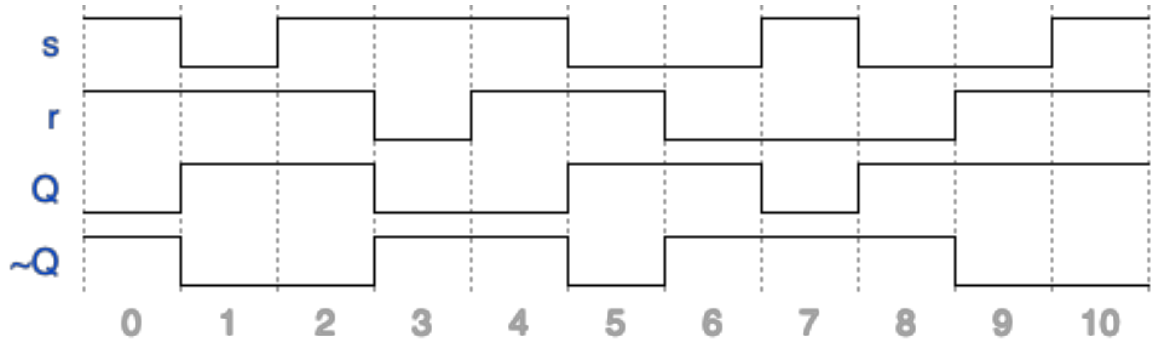
$$\overline{Q} = \overline{r\,\overline{\overline{q}\,\overline{s}}}$$

$$Q = \overline{\overline{q\,\overline{r}\,\overline{s}}}$$

With those we proceeded to building the circuit.



When testing the circuit, this is the timing diagram we've observed:



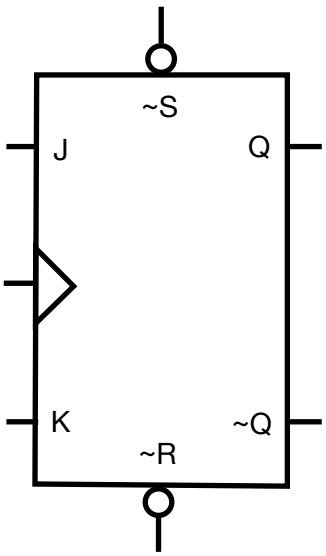
In state 6 we can see, that while there is no signal on either *s* or *r*, the output remains set. What was unexpected though, is the fact that not only was *Q* set, but so was *~Q*. This is natural behaviour for NAND gates, which are both provided with '0' on input, but an undefined state for SR latch.

Task 3

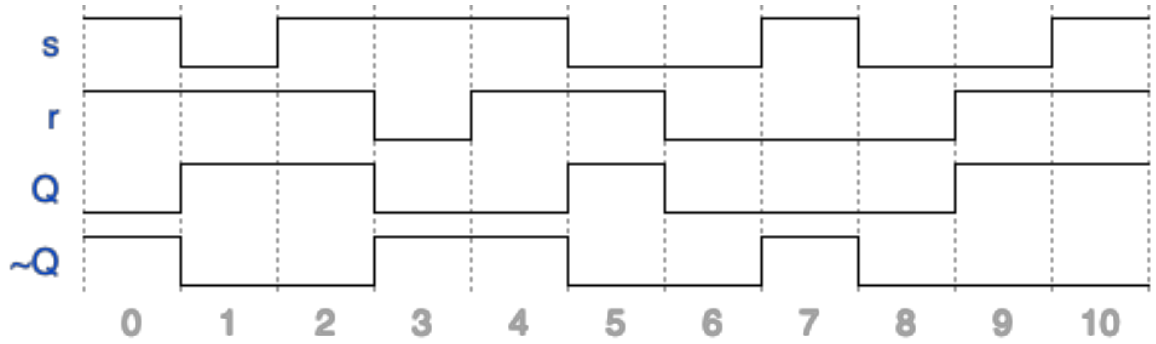
Use only asynchronous inputs of the synchronous D flip-flop to determine their active value and which of them is dominant. Draw timing diagrams used to resolve the problem.

Our method:

We've used the JK gate available in the lab, with J, K, ~S and ~R inputs. Leaving J and K floating, we plugged ~S and ~R to respective buttons' negated output.



When testing different input combinations, this is the timing diagram we saw:



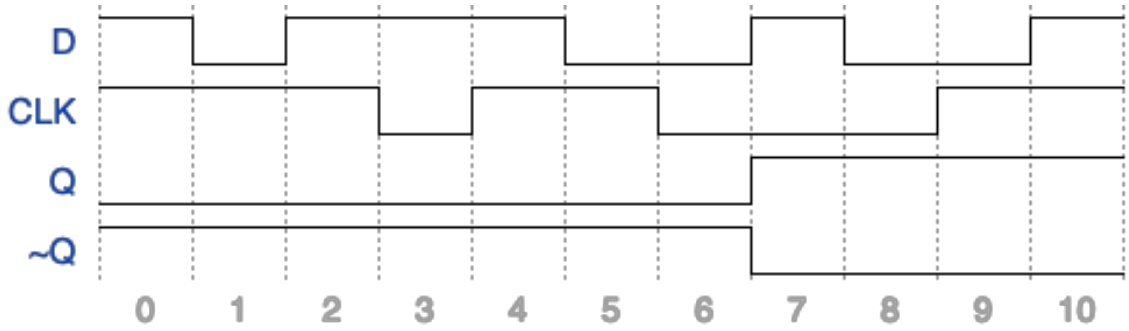
Here, we can notice the reaction opposite to the SR gate from the first task. When both inputs are absent, the *Q*, as well as *~Q* are '0'. This means that JK's asynchronous inputs are reset-dominant.

Task 5

Recognise the triggering way of the synchronous D flip-flops (gated latch, master slave with or without 1s and 0s catching, or positive or negative edge-triggered). Draw timing diagrams used to resolve the problem.

Our method:

While inspecting the D gate, we run the same input combination as in previous tasks on it, in order to determine the triggering way. This is what we observed:



From this diagram, we can evaluate that **D gate is triggered by the CLK's rising edge**. On such occurrence, it reads the state of D input and rewrites it to Q, until next CLK's rising edge.