Theory of Logic Circuits

Laboratory manual

Exercise 3

Bistable devices

1. Classification of bistable devices

A bistable element of flip-flop is a sequential logic device that has two and only two stable output states. In general bistable elements can be divided into two categories:

1. asynchronous devices (called basic latches)
2. synchronous devices.

In turn, synchronous bistable devices can be classified according to the triggering way into three groups:

1. gated latches,
2. master-slave flip-flops (called also pulse-triggered ones),
3. edge-triggered flip-flops.

Also asynchronous devices can be further divided into two groups: fundamental mode (or static) devices and pulse mode (or dynamic) ones. However, since we will not deal with the second group at all, unless explicitly specified, all devices referred to as asynchronous are in fact asynchronous fundamental mode ones.

Flip-flops in each category can be built as devices of type SR, D, JK and T according to the logical functions that they perform. The most often their logical behavior is specified by reduced characteristic tables and by excitation tables. We assume that for assignment of asynchronous flip-flops the lower case letters will be used. For assignment of synchronous ones, we will use capital letters. It should be stressed here that despite of theoretical possibility of building all types of flip-flops as devices of each mentioned category, not all of them have practical meaning due to their bad functionality. For example asynchronous static t flip-flop would not achieve stable state for input t = 1 and output Q of asynchronous static d flip-flop would be always equal to its input. It is self evident that using such elements is senseless.

1.1. Reduced characteristic tables

Reduced characteristic tables present the information about the behavior of the flip-flop for given conditions on its input signals.

S	R	Q^{n+1}	Operation
0	0	Q^n	no change
0	1	0	reset
1	0	1	set
1	1	X	not normally allowed

T	Q^{n+1}	Operation
0	Q^n	no change
1	$\overline{Q^n}$	toggle

J	K	Q^{n+1}	Operation
0	0	Q^n	no change
0	1	0	reset
1	0	1	set
1	1	$\overline{Q^n}$	toggle

D	Q^{n+1}	Operation
0	0	reset
1	1	set

1.2. Excitation tables

Excitation tables gives the information about the desired values on inputs of flip-flop for given transition from present to next state

Q^n	Q^{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Q^n	Q^{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Q^n	Q^{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Q^n	Q^{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

2. Asynchronous flip-flops

In practice only sr flip-flops (and their modifications, like: ~s~r flip-flops) are built as asynchronous devices[1].   First let us consider sr basic latch implemented with the use of two NOR gates (Fig. 1).
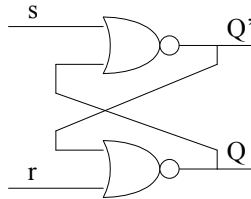

Figure 1. Logic diagram of the NOR-based sr basic latch

The logical symbol of this bistable device is given in the Fig.2. Numbers associated with s, r and Q are connected with the problem of dominance of inputs.
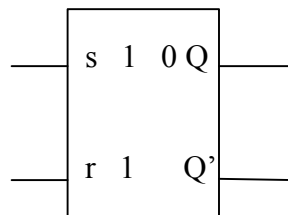

Figure 2. Logic symbol of the sr basic latch with dominant resetting input

It should be taken in account that Q' = ~Q only when two inputs s and r are not active at the same time (active means equal to logic one in this case, since numbers associated with s and r are ones). When these inputs are both active, i.e. when sr = 11, then Q' = Q = 0 (zero is associated with Q in Fig. 2). From what was said here, it is obvious that to be able to use the output Q' of sr flip-flop as ~Q it is necessary to ensure at the design stage of the project that condition sr = 11 will never occur. If this is satisfied, then discussed here problem of input dominance is of no importance and the logic symbol of the sr flip-flop is simplified as shown in Fig. 3.

However in detailed analysis of flip-flops, when we treat them as black boxes and from their behavior we want to get to know about them as much as possible, such normally forbidden condition is very important. It is so important, because it is easy to be recognized, since it is the only case when two outputs of the sr flip-flop are not complementing each other. Therefore after detecting this state we can uniquely determine the active values of inputs. They are the values that cause this normally forbidden state to occur. If they are 11 then we have sr flip-flop and if they are 00 then we have ~s~r.

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[1] The tilde sign "~" preceding the Boolean variable has the meaning that this variable is accessible in complemented form. In other words tilde with some literal creates a name of some other literal. Of course logical value of this new literal is a complement of the literal without tilde. But since tilde is an inherent part of a name it cannot be canceled (according to double complement theorem) if the name with tilde is complemented. For example ~s is abbreviated name of the name COMPLEMENTED_SET_INPUT of the flip-flop. It means that purpose of this input is to set flip-flop, but the active value (value used for performing action) is logic zero.
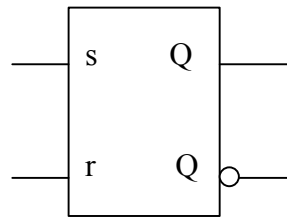
Figure 3. Logic symbol of the sr basic latch

Besides, having detected this state, we can also determine the dominance of inputs. The setting input s (or ~s) is dominant if and only if in normally forbidden state two outputs are equal to logic one. Similarly, the resetting input r (or ~r) is dominant if and only if in normally forbidden state two outputs are equal to logic zero. Therefore if we find that Q = Q' = 0, then the resetting input prevailed over setting one, so it is the flip-flop with dominant resetting input. On contrary, if Q = Q' = 1, then the setting input prevailed over resetting one, so it is the flip-flop with dominant setting input.

It is easy to see, that flip-flop from the Fig. 1 and 2 is the one with dominant resetting input, since when sr = 11 (both active), Q = Q' = 0.

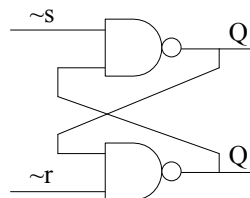Fig. 4 presents NAND-based ~s~r flip-flop with dominant setting input (i.e. for active inputs ~s~r = 00, Q = Q' = 1).

Figure 4. Logic diagram of the NAND-based ~s~r basic latch

Fig. 5 gives the logic symbol of the circuit from Fig. 4. Since it is flip-flop with dominant setting input, the number associated with output Q is 1. The fact that inputs are active low is signaled by dots preceding internal s and r signals. It means that the device has to be connected to external ~s and ~r signals respectively.

Fig.6 presents simplified logic symbol of the ~s~r flip-flop. Such logic symbol can be used in designs only with the restrictions concerning the avoidance of simultaneous active inputs. These restrictions are of the same nature as those discussed earlier for Fig. 2 and Fig. 3.
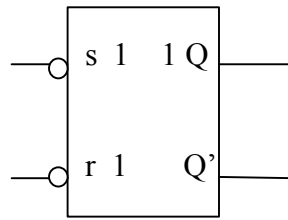
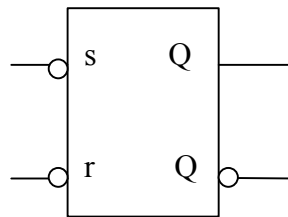Figure 5. Logic symbol of the ~s~r basic latch with dominant setting input

Figure 6. Logic symbol of the ~s~r basic latch

3. Synchronous flip-flops

Synchronous flip-flops will be presented in three subsequent sections. The division into them is made according to different way of triggering. All bistable devices use previously discussed sr basic latch as the fundamental structure to build more complicated circuits.

3.1. Gated latches

The example of gated SR NOR-based latch is given in the Fig.6. When the control input signal C (called clock signal) is 0, signals applied to the S and R inputs can not effect the cross-coupled NOR latch circuit. However, when the clock signal C is 1, signals applied to the S and R inputs can effect the cross-coupled NOR latch circuit.
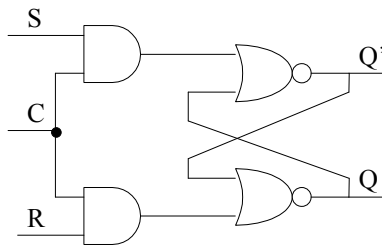
Figure 7. Gated SR NOR-based latch

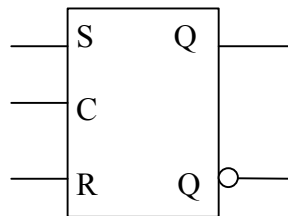The logic symbol of the gated SR latch is provided in Fig. 8.

Figure 8. Logic symbol of the gated SR latch

A gated SR latch can converted to a gated D latch by simple addition of an Inverter as shown in Fig. 9
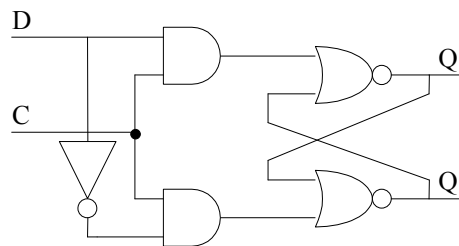

Figure 9. Gated D latch

The Inverter in the gated D latch serves two different purposes. It provides a latch circuit with only one input (not including the clock) called data input. It also insures that SR latch inputs are always complemented so that the signal conditions SR = 11 cannot occur. All gated latches have got the property of transparency. The transparency property simply means that the outputs respond to an input signal change when the control input signal is 1. For gated D latch, the data input signal D is transferred to the Q output when control input signal is 1. The output Q signal follows the data input signal D as long as the control input remains a logic 1. Logic symbol of the gated D latch is given in Fig. 10.
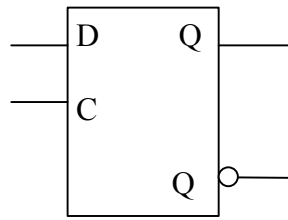
Figure 10. Logic symbol of the gated D latch

3.2. Master-slave flip-flops

A master-slave flip-flop is designed to interrupt the logic connection between the inputs and the outputs during the time the input control signal is a logic 1. Removing the logic connection between the input and output signals afforded by the master-slave design provides the following benefits: it removes the transparency property and hence race condition in feedback applications as well as it provides a memory device, which can be used in synchronous sequential designs. The circuit diagram of the master-slave JK flip-flop shown in Fig. 11. presents how the transparency property is removed by interrupting signal path from the inputs to the outputs.
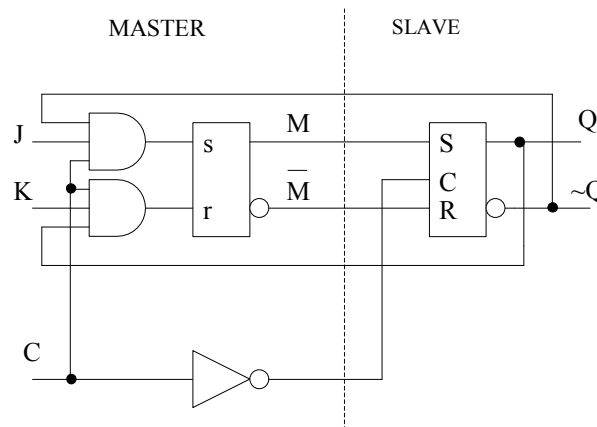

Figure 11. Master-slave (pulse-triggered) JK flip-flop

The master-slave JK flip-flop is simply two gated SR latches connected in cascade such that master drives the slave. The present state outputs of the slave are fed back to the inputs of the master such that the J inputs is qualified by ~QC while K is qualified by QC, providing steering and thus allowing the toggle property. When the external control input signal is a logic 1, the master is transparent from its inputs to its outputs. Because of the Inverter, during this same time period the slave remains stable and cannot cause the race conditions through the slave via the outputs of the master. In effect this interrupts the logic connection between the inputs and the outputs of the device during the time the clock C is a logic 1. When the clock makes a transition from a logic 1 to a logic 0, the data present at the J and K inputs are captured, the master is disabled, and the slave is enabled. Changes at the master's inputs are of no consequence at this

time since it is now disabled and its outputs are stable. The slave is now transparent but the master is supplying it with stable inputs. Master-slave can toggle only once for each external clock signal pulse. Because master-slave utilizes both edges of the external signal applied to clock input, this type of flip-flop is a pulse-triggered one.

Despite of the interrupt in logic connection between master and slave, this type of flip-flops can have drawbacks. The main drawback is 1s catching or 0s catching property. This property is due to the fact that that the master is transparent during the time the external clock is a logic one. Therefore when the slave's output is a logic 0 and J input changes to 1 after rising edge of C, then master will catch this set condition. The set condition is then passed on to the slave on the falling edge of C. The slave's output becomes a logic 1, although on rising edge of the clock J input was inactive. It means that such flip-flop catches 1s. The 0s catching is essentially the same, with the difference that it happens when slave's output is a logic 1 and reset condition on K input occurs after raising edge of the clock. This reset condition is caught by master and then passed on to the slave resetting its output. The 1s catching and 0s catching property exists for all master-slave flip-flops that do not contain data-lockout feature. When data-lockout feature is present, then the input conditions are checked only on raising edge and 1s or 0s catching does not take place. The logic symbol of JK flip-flop with 1s and 0s catching is shown in the Fig. 12, while logic symbol of JK flip-flop with data-lockout is shown in the Fig. 13.
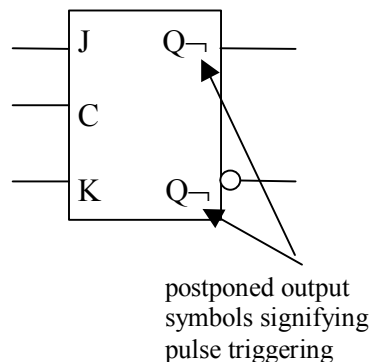

postponed output
symbols signifying
pulse triggering

Figure 12. Logic symbol of the master-slave JK flip-flop with 1s and 0s catching
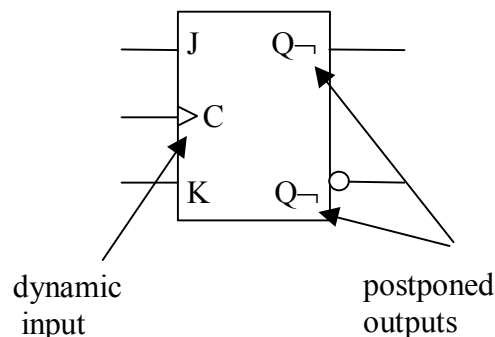

dynamic
input

postponed
outputs

Figure 13. Logic symbol of the master-slave JK flip-flop with data-lockout feature

3.3. Edge triggered flip-flops

An edge-triggered flip-flop is a device designed to respond to a raising or a falling edge of the clock signal. The influence of external signals on inputs and changes on outputs of edge-triggered flip-flops are made on the same edge of the clock. Changes of input signals that occur outside of the very short time (setup time + hold time) around the active edge of the flip-flop are ignored. The logic symbol of positive edge-triggered D flip-flop is given in Fig. 14 and logic symbol of negative edge-triggered D flip-flop is given in Fig. 15.
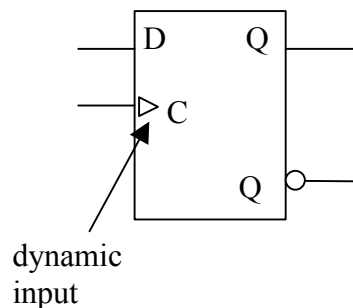

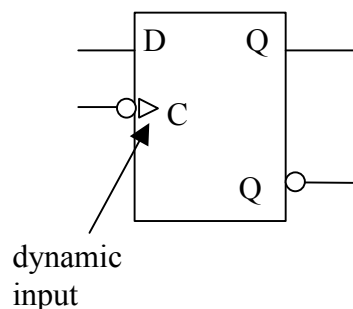Figure 14. Logic symbol of the positive edge-triggered D flip-flop

Figure 15. Logic symbol of the negative edge-triggered D flip-flop

4. How to prepare yourself at home to laboratory

1. You should know the reduced characteristic tables and excitation tables of all types of flip-flops.
2. You should be familiar with terminology and concepts concerning classification of flip-flops, active values and dominance of inputs, the triggering ways.
3. You should resolve all theoretical parts of the tasks below, so that on laboratory, you could implement your designs and verify your ideas. Especially you should have designed on a paper all circuits and prepared (in the form of timing diagrams) such changes of inputs, which after filling outputs (from observations made during laboratory) give you unique answers. My suggestion is to prepare short timings – one waveform for only one question, and not one long waveform suitable for all problems covered in a task.

5. Tasks to be performed during laboratory

1. Design and implement with NAND gates sr basic latch with dominant setting input (Fig. 16). Draw timing diagrams (taken from the built circuit) illustrating the behavior of the device
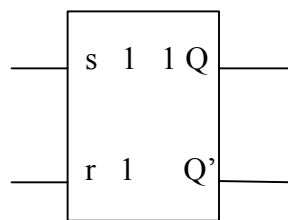

Figure 16. Logic symbol of the sr basic latch with dominant setting input

2. Design and implement with NAND gates ~s~r basic latch with dominant resetting input (Fig. 17). Draw timing diagrams (taken from the built circuit) illustrating the behavior of the device
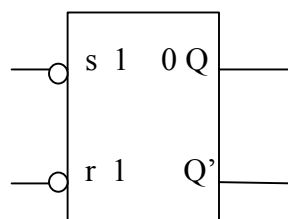

Figure 17. Logic symbol of the ~s~r basic latch with dominant resetting input

3. Use only asynchronous inputs of the synchronous D flip-flop to determine their active value and which of them is dominant. Draw timing diagrams used to resolve the problem
4. Use only asynchronous inputs of the synchronous JK flip-flop to determine their active value and which of them is dominant. Draw timing diagrams used to resolve the problem
5. Recognize the triggering way of the synchronous D flip-flops (gated latch, master slave with or without 1s and 0s catching, or positive or negative edge-triggered). Draw timing diagrams used to resolve the problem

6. Recognize the triggering way of the synchronous JK flip-flops (gated latch, master slave with or without 1s and 0s catching, or positive or negative edge-triggered). Draw timing diagrams used to resolve the problem.
   Help: Since the task here is not to obtain full characteristics of the JK flip-flop, but only the triggering way, it is convenient to connect inputs J and K together. In this way from logical point of view you will obtain T flip-flop, but the triggering way will remain unchanged and the circuit will have only two inputs (T and C) instead three (J, K and C). It will simplify the problem.

6. Instructions to follow

1. Solve all tasks before the exercise.
2. Implement the circuits specified by your supervisor (using given elements).
   Present working circuits to your supervisor for acceptance.