Theory of Logic Circuits

Academic year	Term		Exercise Supervisor	Deans group	Section
2018/2019	Thursday 15:15 – 17:45	Makrokierunek	GKB	1,2	1

Report from exercise number 5

Exercise performed on: 2019-03-14

Subject of the exercise:

Synchronous sequential logic circuits

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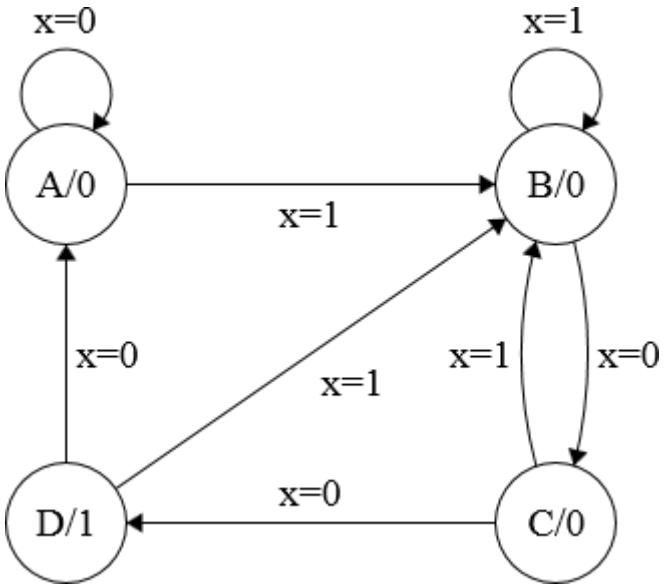
Task 1

Design Moore type synchronous state machine with input X and one output Z. Outputs goes 1 for one clock period when 1-0-0 sequence is detected on input signal X. Draw logic circuits using D flip-flops and describe all necessary steps for solution method. Prepare working model of this machine during labs.

We have started with creating a transition diagram representing how the machine is supposed to work and a timing diagram to simulate its functioning. After that we built an excitation table and Karnaugh maps for the machine's outputs and D flip-flops' inputs. With prepared inputs We were able to derive the equations and, after transforming into NAND gates, implement them into a working model.



State	$x = 0$	$x = 1$	Z	Q_1	Q_2
A	A	B	0	0	0
B	C	B	0	0	1
C	D	B	0	1	0
D	A	B	1	1	1

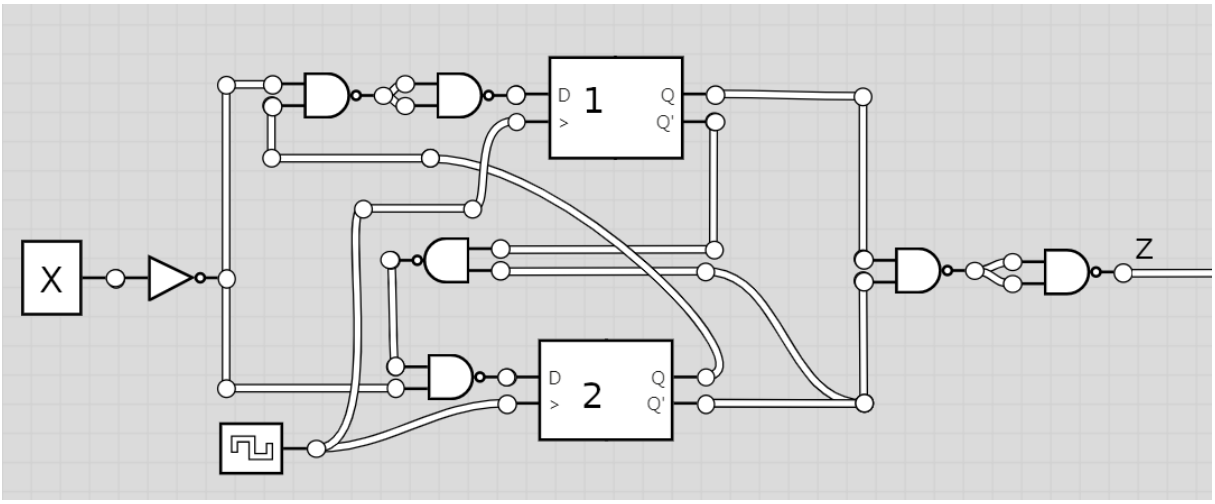
State	$x = 0$	$x = 1$	Z
00	00	01	0
01	11	01	0
10	00	01	0
11	10	01	1

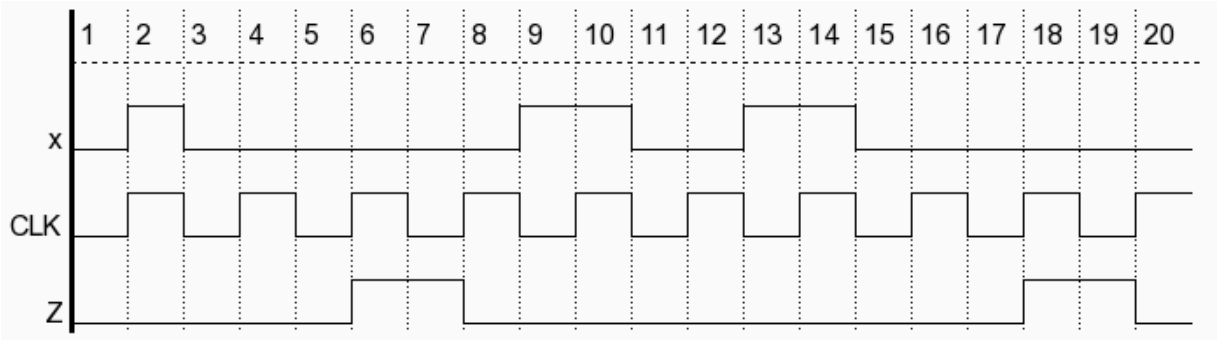
$Q_1Q_2\backslash x$	0	1
00	0	0
01	1	0
11	1	0
10	0	0

D_1

$Q_1Q_2\backslash x$	0	1
00	0	1
01	0	1
11	1	1
10	0	1

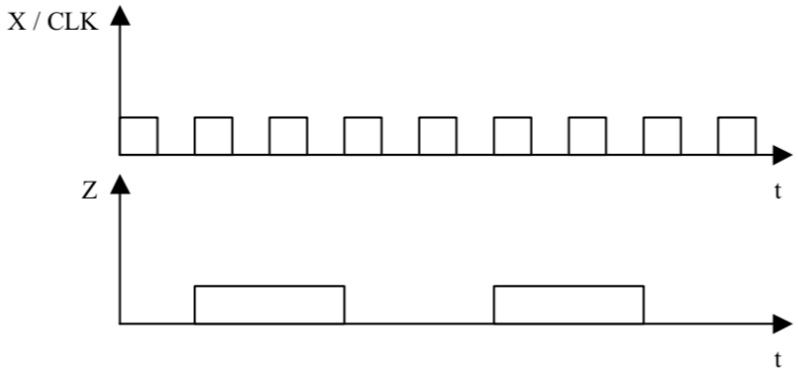
D_2





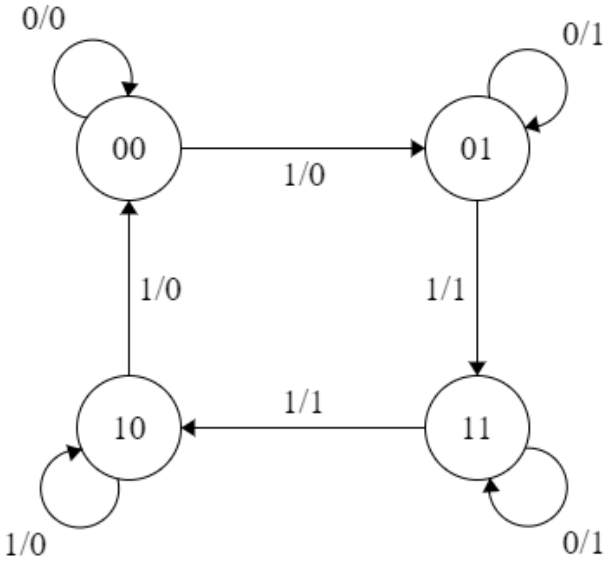
Task 2

Design Mealy type synchronous state machine implementing input signal frequency divider (by 4), as shown on timing diagram. There is CLK input as frequency source and one blocking input X, setting output Z=1 any time, when 1. See timing diagram below:



Draw logic circuits using J-K flip-flops and describe all necessary steps for solution method. Prepare working model of this machine during labs.

This task has been solved using D flip-flops, because there were no available JK gates to our disposal.

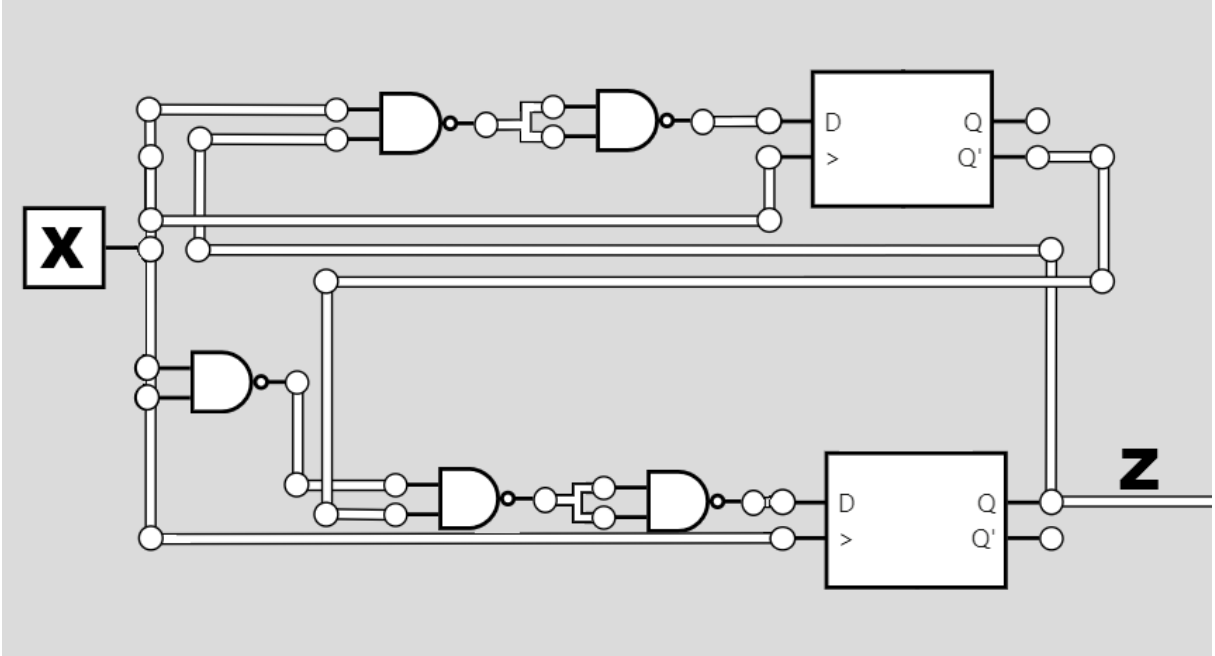


$Q_1Q_2\backslash x$	0	1
00	00	01
01	01	11
11	11	10
10	10	00

Q_1Q_2

$Q_1Q_2\backslash x$	0	1
00	0	0
01	1	1
11	1	1
10	0	0

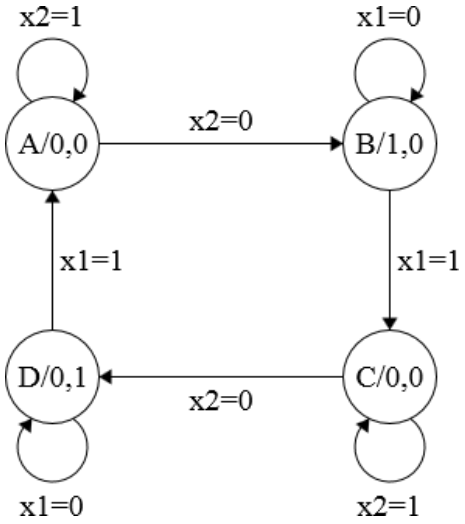
$Z = Q_2$



Task 3

Design a water-pumps tower for a small village. The water can is located at the highest hill and is operated using two water pumps. The water is flowing out of the can with instant, small stream. The can is equipped with two level sensors: high level x1 & low level x2. When the water level reaches low level (x2=0) the first pump shall start operating (P1=1). The pump stream is much bigger than flow-out stream thus single pump can always fill the can. When the water level reaches the high level (x1=1) the system shall switch off the pump (P1=0) and then wait until the water level reaches again low level (x2=0), then shall start pumping water again using second pump (P2=1). When the water level reaches the high level (x1=1) the system shall switch off the pump and the process repeats. Draw circuit using D f-f, draw circuit using JK f-f.

We've started with preparing a timing and state diagrams of the machine. Then, we obtained composite K-Maps for the next state inputs and external outputs. With ready Karnaugh Maps we derived the equations for the J-K flip-flops and built a working model of this machine using NAND gates.



State	$Q_1; Q_2$	$x_1 = 0; x_2 = 0$	$x_1 = 0; x_2 = 1$	$x_1 = 1; x_2 = 1$	$x_1 = 1; x_2 = 0$	$P1; P2$
A	00	B	A	A	B	00
B	01	B	B	C	C	10
C	11	D	C	C	D	00
D	10	D	D	A	A	01

$Q_1Q_2\backslash x_1x_2$	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	1	1	1	1
10	1	1	0	0

D_1

$Q_1Q_2\backslash x_1x_2$	00	01	11	10
00	1	0	0	1
01	1	1	1	1
11	0	1	1	0
10	0	0	0	0

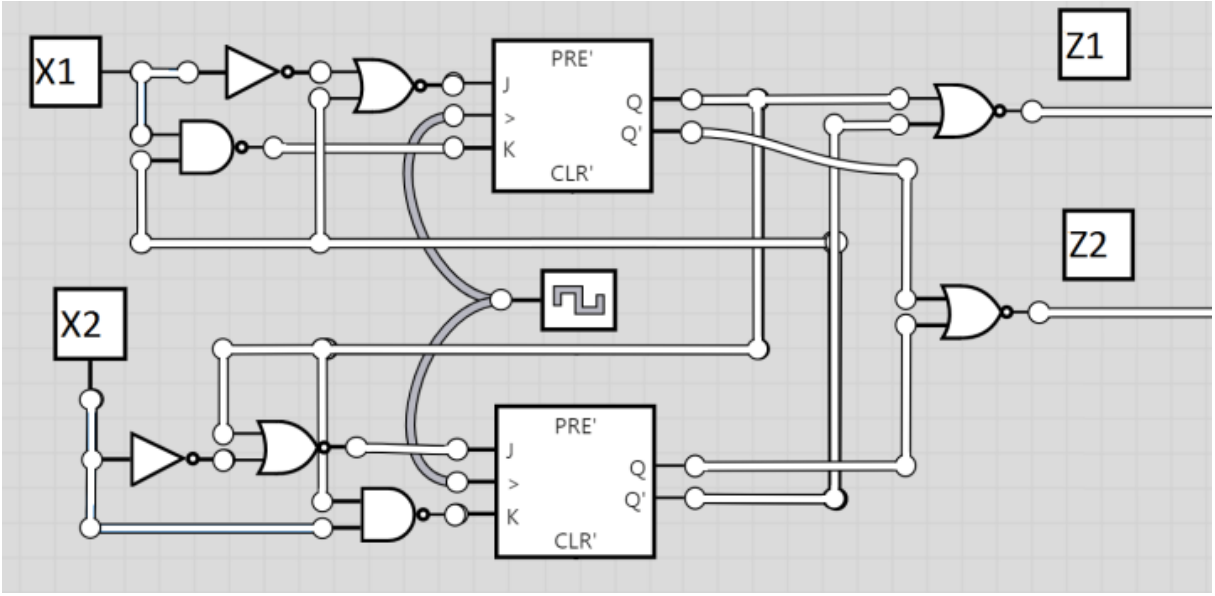
D_2

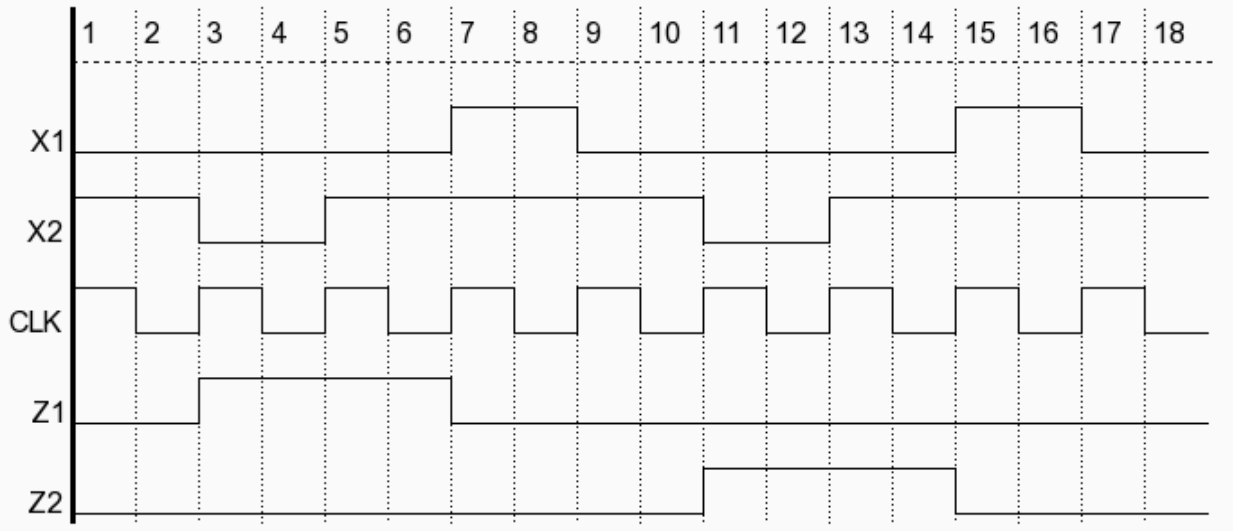
$$D_1 = \overline{x_1}Q_1 + x_1Q_2 + \overline{Q_1}Q_2 \qquad J_1 = x_1Q_2$$

$$D_2 = \overline{x_2}\overline{Q_1} + x_2Q_2 + Q_1Q_2 \qquad K_1 = x_1\overline{Q_2}$$

$$P_1 = \overline{Q_1}Q_2 \qquad J_2 = \overline{x_2}\overline{Q_1}$$

$$P_2 = Q_1\overline{Q_2} \qquad K_2 = \overline{x_2}Q_1$$


X1
X2
Z1
Z2
PRE'
J
>
K
Q
Q'
CLR'
PRE'
J
>
K
Q
Q'
CLR'


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
X1
X2
CLK
Z1
Z2