Theory of Logic Circuits

Laboratory manual

Exercise 5

Synchronous sequential logic circuits

1. Introduction.

1.1. Moore & Mealy Type Synchronous State Machines

Synchronous state machine is the one, where its internal state changes along with synchronous input C (clock) or CLK. Typically C has rectangle waveform. State usually changes on arising or falling edge of clock signal (Edge-Triggered Devices).

Synchronous sequential circuits can be Moore or Mealy type state machines.
The main difference is its output method. In Moore type circuit outputs are dependent on only the present state of the circuit, as shown on Fig. 1.

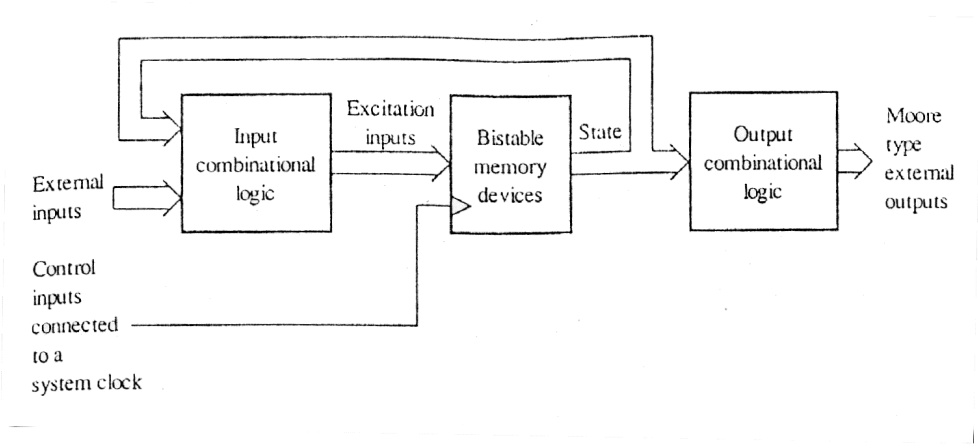


Fig. 1 Moore type circuit

In Mealy type circuit outputs are dependent on both the external inputs and present state of the circuit, as shown on Fig. 2.

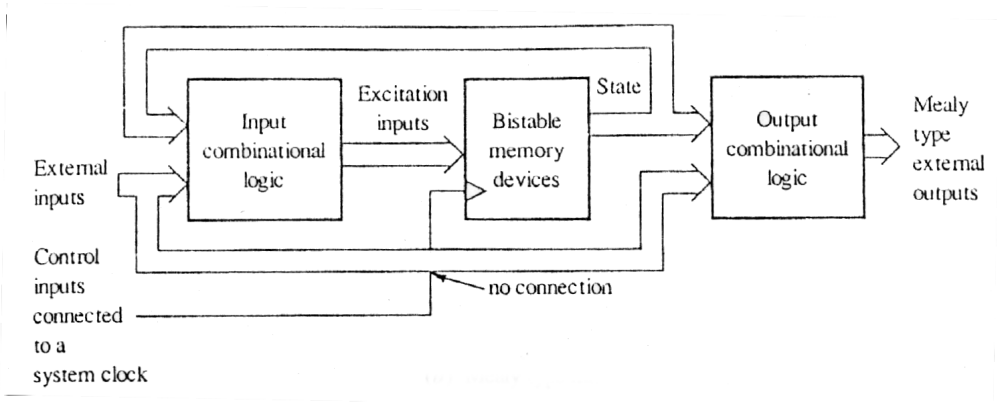


Fig. 2 Mealy type circuit

There can be mixed type circuit with both Moore and Mealy type outputs, as well.

2. Synchronous design process

Typical synchronous design process can fit into 6 main steps:

- Organize design specification, typically into state diagram, PS/NS table, ASM chart or timing diagram.
- Perform state reduction to achieve fewer flip-flops.
- Determine minimum number of flip-flops and assign state variables. Remember that optimal state variable assignment can reduce output combinational logic.
- Select type of flip-flops, then determine its excitation input equations and output equations.
- Draw synchronous sequential logic circuit diagram.
- Prepare working model during labs.

2.1. Example

Design a Moore type synchronous state machine with two external inputs X1, X2 and one output Z. Z goes 1 when X1*(~X2)=1[1] at the next system clock timing event. The output stays at 1 as long as X2=0 otherwise, the output goes to 0. All flip-flops are rising edge driven. Solve the problem using selected method, then draw a circuit for this example.

Sample timing diagram shown below, represents typical working situation for the circuit. See output Z goes 1, when X_1=1 and X_2=0. Because this is synchronous model, this circuit "see" the change when next timing even occurs (as dashed line follows).

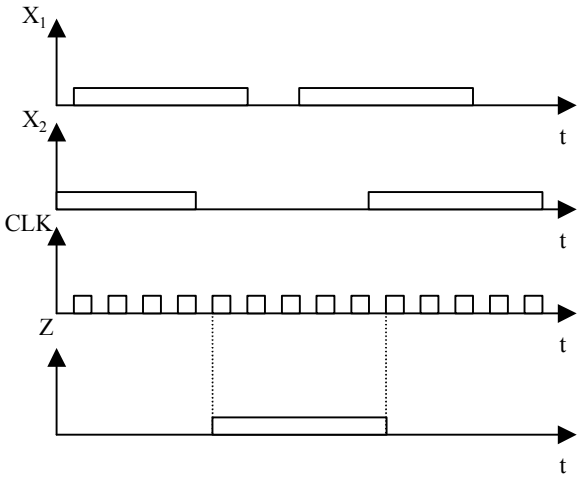


Fig. 3 Timing diagram

State diagram for the machine is represented on Fig. 4. There are only two states for this example, so only one flip-flop is needed to complete this task.

[1] The ~ (tilde) represents complement operator.

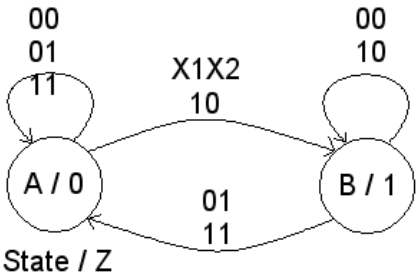


Fig. 4 State diagram (state machine)

A state map can be drawn now:

X_1X_2	00	01	11	10	Z
A	A	A	A	B	0
B	B	A	A	B	1

Fig. 5 State map w/output Z

The system clock signal is implied; therefore, it is not shown in the composite Karnaugh map.

Notice, that it is possible to reduce output combinational logic by assigning internal states equal to output Z.
Following state assignment guarantees optimal output logic:

A=0
B=1

There is no state reduction possible for this example.
Because of assignment, we obtain equation for output Z:

Z=Y

Using state assignment we get following Karnaugh map.

X_1X_2	00	01	11	10	Z
y 0=A	0	0	0	1	0
1=B	1	0	0	1	1
				Y	

Fig. 6 Karnaugh map w/output

In terms of the present state variable y and the next state variable Y we obtain:
$Y = X_1(\sim X_2) + (\sim X_2)y$

During next step we obtain excitation inputs for selected flip-flops.

Now we decide to draw the circuit using D type flip-flops and then J-K flip-flops.

Only one flip-flop is needed.
We mark bold all cells, where y→Y changes (1→0 or 1→0).

$X_1^t X_2^t$	00	01	11	10
y 0	0	0	0	**1**
1	1	**0**	**0**	1

Y

Fig. 7 Karnaugh map for D flip-flop

For D-type flip-flops we obtain following excitation input D equation:
$D = X_1(\sim X_2) + (\sim X_2)Y$
For J-K flip-flops we obtain excitation input maps, as shown below.
Notice that using PS/NS table for J-K flip-flops, we get following Karnaugh maps for both J and K inputs:

$X_1^t X_2^t$	00	01	11	10
y 0	0	0	0	**1**
1	-	-	-	-

J^t

$X_1^t X_2^t$	00	01	11	10
y 0	-	-	-	-
1	1	**0**	**0**	1

K^t

Fig. 8 Karnaugh map for J-K flip-flop

We get excitation input J and K equations:

$J=X_1(\sim X_2)$
$K=\sim X_2$

Notice there is no external loop-back signal. Excitation inputs J and K are not dependent on current internal state for this state machine.

For T flip-flops there is simple rule:

T=1 for all cells (Karnaugh map Fig. 7) where bold 0s or 1s are.
T=0 for all other cells in Karnaugh map.

Using rule above, we obtain Karnaugh map for T flip-flop:

X_1^t / X_2^t	00	01	11	10
y 0	0	0	0	**1**
1	0	**1**	**1**	0

Y

Fig. 9 Karnaugh map for T flip-flop

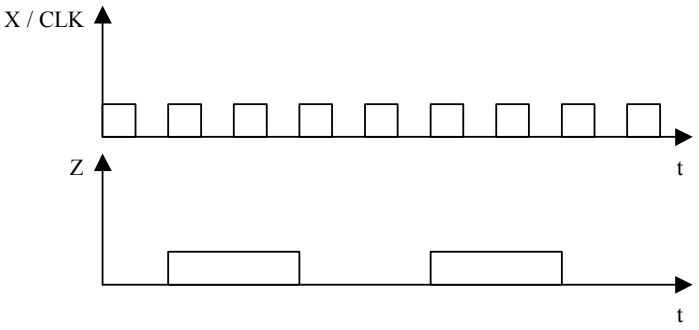
We get excitation input T equation:

$T=yX_2+(\sim y)X_1(\sim X_2)$

3. Tasks to be performed during laboratory

1. Design Moore type synchronous state machine with one input X and one output Z.
   Output goes 1 for one clock period, when 1 – 0 – 0 sequence is detected on input signal X.
   Draw logic circuits using D flip-flops and describe all necessary steps for solution method.
   Prepare working model of this machine during labs.

2. Design Mealy type synchronous state machine implementing input signal frequency divider (by 4), as shown on timing diagram. There is CLK input as frequency source and one blocking input X, setting output Z=1 any time, when 1. See timing diagram below:



   Draw logic circuits using J-K flip-flops and describe all necessary steps for solution method.
   Prepare working model of this machine during labs.

3. Design a water-pumps tower for a small village. The water can is located at the highest hill and is operated using two water pumps. The water is flowing out of the can with instant, small stream. The can is equipped with two level sensors: high level x_1 & low level x_2. When the water level reaches low level (x_2=0) the first pump shall start operating (P_1=1). The pump stream is much bigger than flow-out stream thus single pump can always fill the can. When the water level reaches the high level (x_1=1) the system shall switch off the pump (P_1=0) and then wait until the water level reaches again low level (x_2=0), than shall start pumping water again using second pump (P_2=1). When the water level reaches the high level (x_1=1) the system shall switch off the pump and the process repeats. Draw circuit using D f-f, draw circuit using JK f-f.

4. Instructions to follow

1. Solve all tasks before the exercise.
2. Implement the circuits specified by your supervisor (using given elements).
3. Present working circuits to your supervisor for acceptance.