Theory of Logic Circuits					
Academic year	Term	Makrokierunek	Exercise Supervisor	Group	Section
2018/2019	Thursday 15:15-16:45		KP	3	1

Report from exercise number 6

Exercise performed on: 2019-05-30

Subject of the exercise:
Selected arithmetic switching circuits

Section consists of:

Mikołaj Dobosz
Wojciech Bieniek

Task 1

Implement 1-bit full serial adder using NAND gates and D flip flop.

C_i	A_i	B_i	C_{i+1}	S_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

AB\C	0	1
00	0	0
01	0	1
11	1	1
10	0	1

C_{i+1}

AB\C	0	1
00	0	1
01	1	0
11	0	1
10	1	0

S_i