Theory of Logic Circuits

Laboratory manual

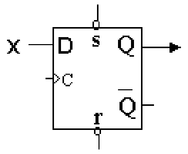
Exercise 9

Registers

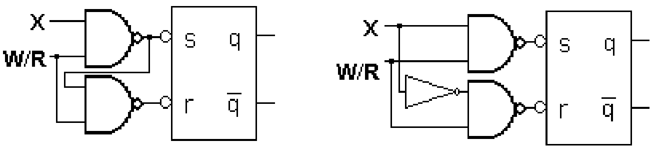
1. Introduction

Registers are such sequential circuits that their purpose is storing information. The main parameters that characterise a register are its length (equal to the number of flip-flops used in the construction) and the way of first loading data into it, then reading it.

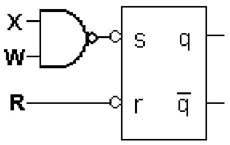
If for loading data to a register there are used information inputs of flip-flops (such as D, JK) then it is synchronous loading as it happens on an active edge of a clock signal.



If there are used setting and resetting inputs sr we talk about asynchronous loading of information. Asynchronous loading may be done in two ways: in one stage when flip-flops are set or reset accordingly to the incoming data, or in two stages. Then the first is resetting of the whole register, the second setting only these flip-flops that correspond to the incoming 1s.



Loading in one stage



Loading in two stages

We usually assume that sr inputs are active with “0” (which also helps us using synchronous flip-flops as we may use their asynchronous inputs).

It is essential to establish the meaning of values of such auxiliary signals as W/R, W, R. For loading in a single stage when W/R=0 then the writing to a register is performed, when it is 1 we may read the information stored. For loading in two stages accordingly to the implementation given above, to write we should have first R=0 to reset the register, then it should become inactive (R=1) and after setting the new values of data bits W should go to one to load the information. For reading we use the phase of inactivity on both W and R, W=0 and R=1.

Writing data to a register requires some time. When this time depends on a number of bits of data then it corresponds to serial loading of information as only then the circuit needs as many clock periods as many there are flip-flops used. Such registers are called shift registers as they shift the data between flip-flops.
When the time of loading information is constant and independent of the length of a register, then writing data to it must be done in parallel – i.e. to each flip-flop separately.
Reading information from a register also may be achieved in a serial or parallel way.

That leads to four categories of registers:

- Parallel-in parallel-out,
- Parallel-in serial-out,
- Serial-in parallel-out,
- Serial-in serial-out.

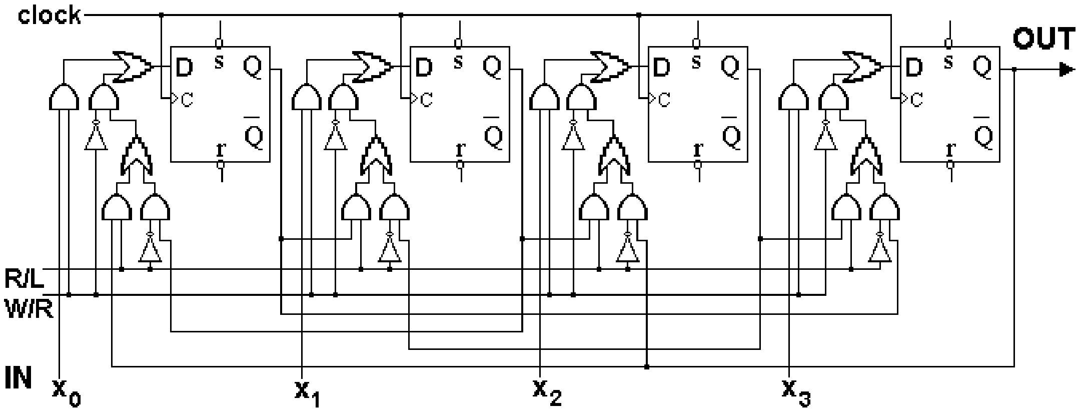
The first type registers are often simply called parallel ones while the others are shift registers, mentioned above.
If loading of information happens in parallel, it may be either synchronous or asynchronous, but when it is serial then it should be synchronous (only this type allows for shifting information).
The simplest shift registers shift in one direction, more complicated (which require some additional elements apart from flip-flops) may change directions as shown below in an example.

2. Example

Draw a logical diagram of a bi-directional 4-bit parallel-in serial-out register with synchronous loading of data, which does not loose information at the stage of reading.

First we need to think what function we should feed into *n*-bit of this register. We will need two additional signals apart from data signals. One for indicating the stage of loading or reading (shifting) data – W/R (W/R=1 means writing, W/R=0 means reading), and the other for indicating the direction of shifting – R/L (R/L=1 means shifting right, R/L=0 means shifting left).

Then the function is $D_n = W/R \cdot x_n + \overline{W/R} \cdot (R/L \cdot Q_{n-1} + \overline{R/L} \cdot Q_{n+1})$ and the diagram as follows.



There is also a group of circuits called shift register counters. They consist of a shift register but with a backward loop of some kind. Dependent on the function used in this feedback loop we have three classes of such shift register counters:

- Ring counters,
- Twisted ring counters (Johnson counters),
- Maximum length shift registers.

Ring counters simply feed the first flip-flop with the signal coming out of the last flip-flop. Such register counters may be used to obtain the effect of a "circling 1" or "0". For "circling 1" with self-correction the function for the backward loop should be as follows:

$$x_0 = \overline{Q_0^t + Q_1^t + \ldots + Q_n^t + \ldots + Q_{N-2}^t}$$

For circling "0" with self-correction the feedback loop function for the first flip-flop should be:

$$x_0 = \overline{Q_0^t \cdot Q_1^t \cdot \ldots \cdot Q_n^t \cdot \ldots \cdot Q_{N-2}^t}$$

Basic structure (without self-correction mechanism) of the twisted ring counter is designed by feeding the first flip-flop with the inversion on the last flip-flop output signal, but then it is necessary to hand-set the starting conditions for a register. Without this, the register just shifts information that was stored in flip-flops, which may be not what is expected to be there.

Maximum length shift register counter has the first flip-flop fed with the result of XOR operation performed on the two the most significant bits.

3. Tasks to be performed during laboratory

1. Design a 4-bit parallel-in serial-out register with synchronous loading of data, not loosing information at the stage of reading.
2. Design a 4-bit shift register counter with the effect of "circling 1" providing it with synchronous self-correction mechanism.
3. Design a 4-bit parallel-in parallel-out register with loading information in one asynchronous stage.
4. Design a 4-bit maximum length shift register counter.

For all tasks given, the available logical elements are D and JK flip-flops, 2- and 4-input NAND gates, 2-input NOR gates, 2-input XOR gates.

4. Instructions to follow

1. Solve all tasks before the exercise.
2. Implement the circuits specified by your supervisor (using given elements).
3. Present working circuits to your supervisor for acceptance.