Theory of Logic Circuits					
Academic year	Term	Makrokierunek	Exercise Supervisor	Group	Section
2018/2019	Thursday 15:15-16:45		KP	2	1

Report from exercise number 9

Exercise performed on: 2019-05-09

Subject of the exercise:

Registers

Section consists of:

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Task 1

Design a 3-bit shift register counter with the effect of "circling 0" providing it with synchronous self-correction mechanism.

We created truth table for X (input of 1st flip-flop):

$Q_3\ Q_2\ Q_1$	**X** (only allowed states)	X (with self-correction)
0 0 0	-	1
0 0 1	-	1
0 1 0	-	1
0 1 1	1	1
1 0 0	-	1
1 0 1	1	1
1 1 0	0	0
1 1 1	-	0

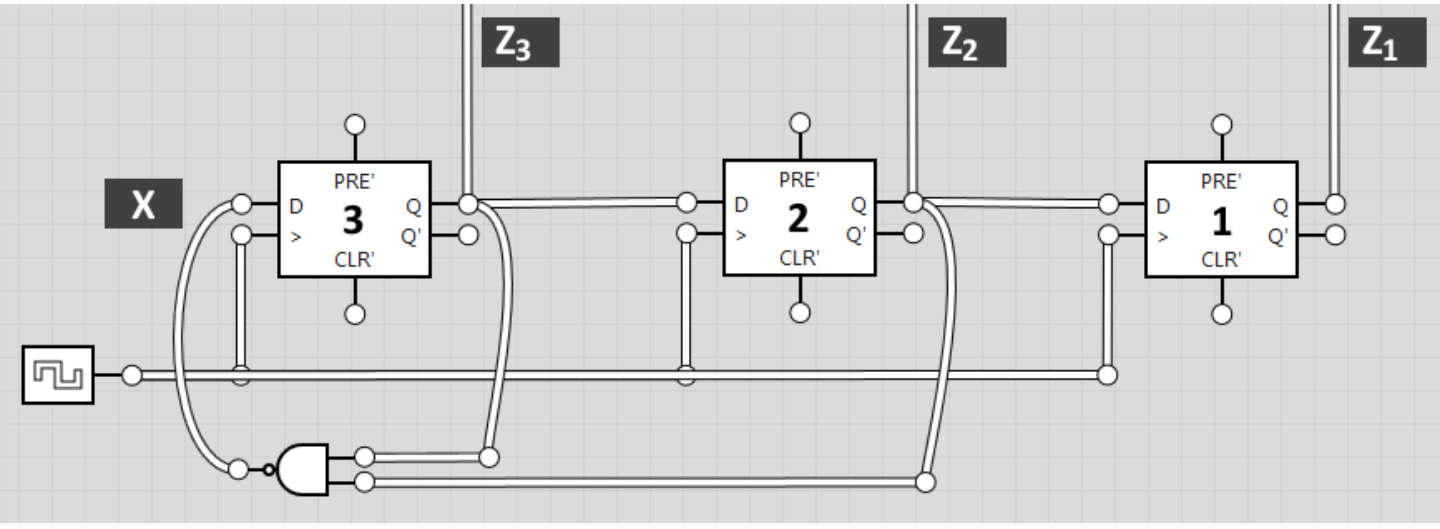
Later we prepared Karnaugh map for X:

Q_3 \ $Q_2\ Q_1$	**0 0**	**0 1**	**1 1**	**1 0**
0	1	1	1	1
1	1	1	0	0

We derived equation and converted it to NAND gate:

$$X = \overline{Q_3} + \overline{Q_2} = \overline{Q_3 \cdot Q_2}$$

And implemented into our device:



Task 2

Design a 3-bit parallel-in serial-out register with loading information in one asynchronous stage, not loosing information at the stage of reading.

We created parallel writing for asynchronous inputs by simply connecting W with X_i (for preset) and $\sim X_i$ (for reset). Then we designed a loop for serial reading of the data, connecting R with previous Q.