Theory of Logic Circuits					
Academic year	Term	Makrokierunek	Exercice Supervisor	Group	Section
2018/2019	Thursday 15:15 - 16:45		KP	3	2

Report from exercice number 9

Exercice performed on 2019-05-09

Subject of the excercise:

Registers

Section consists of:

- Wojciech Bieniek
- Mikołaj Dobosz

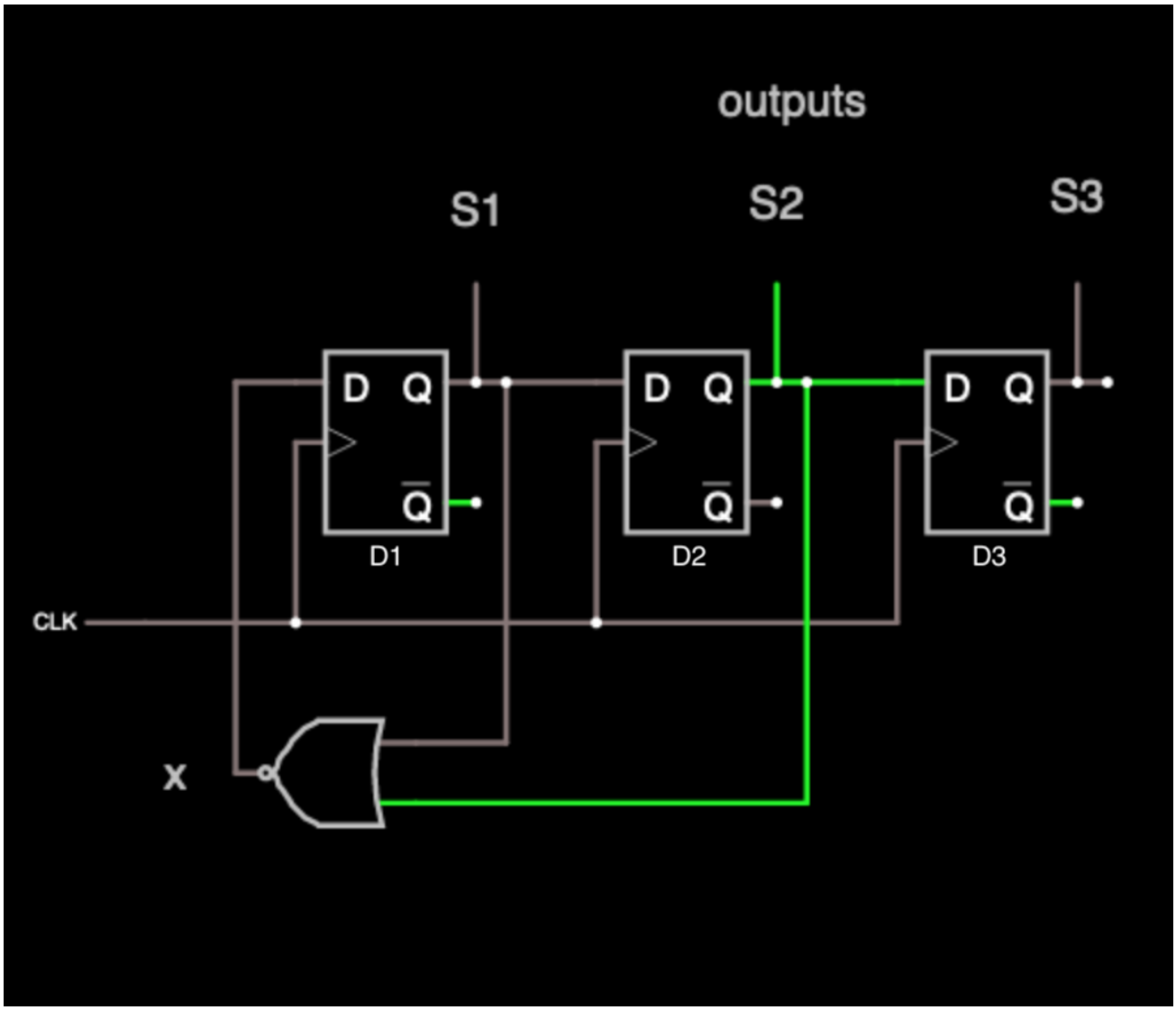
Task 1

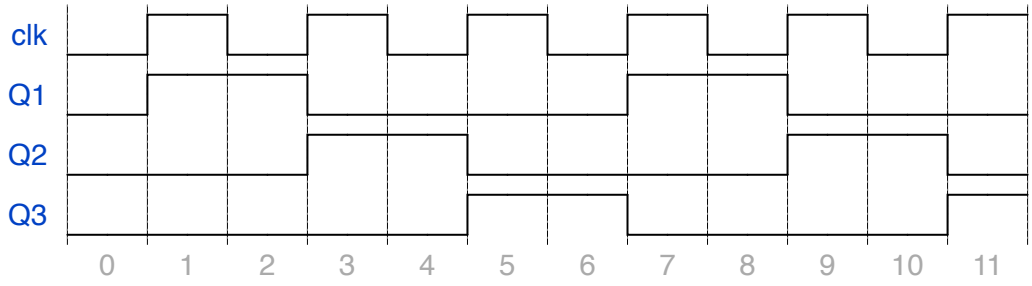
Design and build a 3-bit shift register with a circling “1” and synchronous self-correction. Provide K-map, truth table and a timing diagram.

Q_1	Q_2	Q_3	S
0	0	0	**1**
0	0	**1**	**1**
0	**1**	0	0
0	**1**	**1**	0
1	0	0	0
1	0	**1**	0
1	**1**	0	0
1	**1**	**1**	0

$Q_1 \setminus Q_2\, Q_3$	00	01	11	10
0	1	1	0	0
1	0	0	0	0

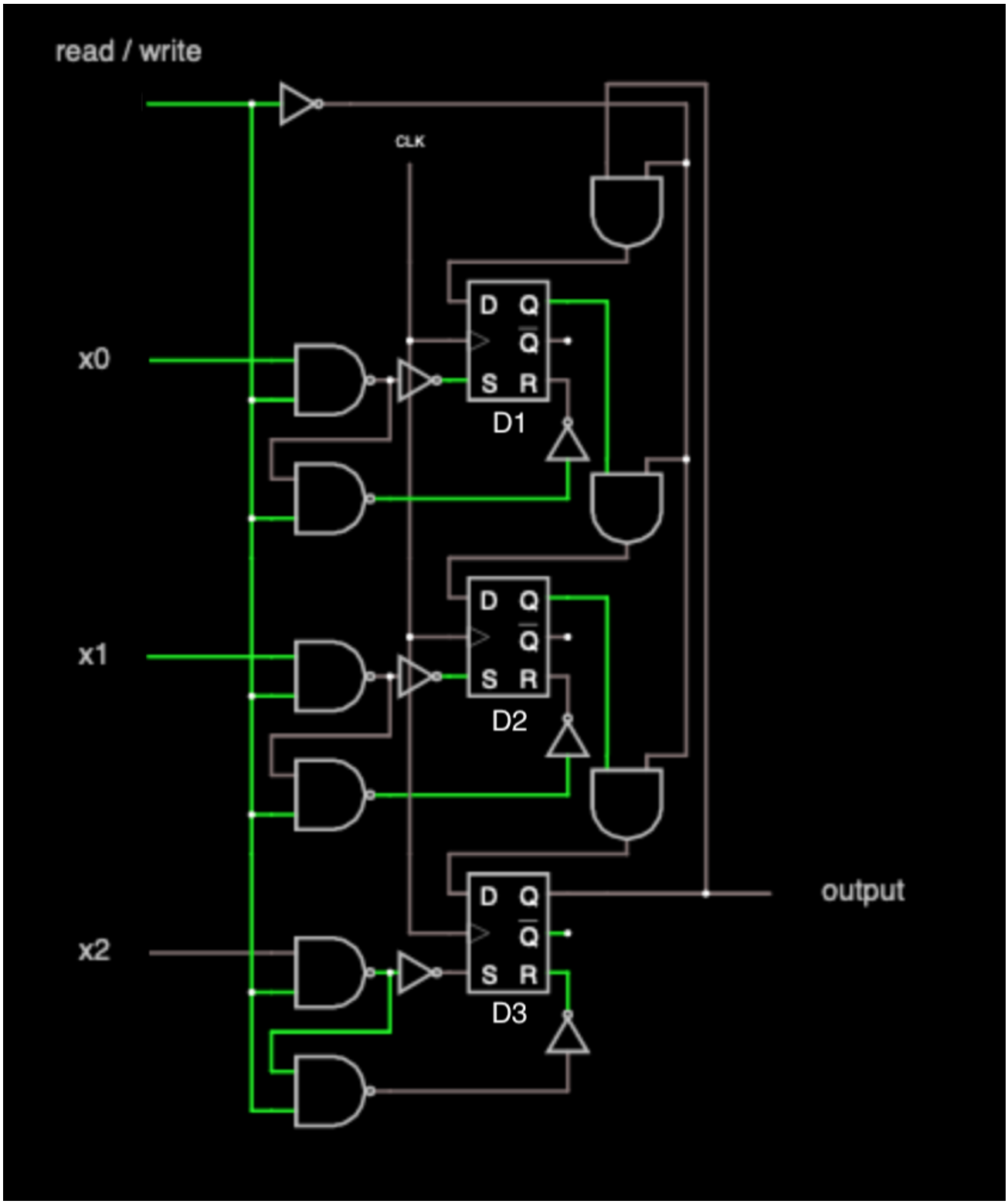
$$S = \overline{Q_1} * \overline{Q_2} = \overline{Q_1 + Q_2}$$





Task 2

Design a 3-bit parallel-in serial-out register with loading information in one asynchronous stage, not loosing information at the stage of reading.


read / write
CLK
x0
x1
x2
D Q
Q
S R
D1
D2
D3
output